Duke University
Edmund T. Pratt, Jr. School of Engineering

ECE 141 Spring 2007
Test III
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Name (please print)_____

In keeping with the Community Standard, I have neither provided nor received any assistance on this test. I understand if it is later determined that I gave or received assistance, I will be brought before the Undergraduate Judicial Board and, if found responsible for academic dishonesty or academic contempt, fail the class. I also understand that I am not allowed to speak to anyone except the instructor about any aspect of this test until the instructor announces it is allowed. I understand if it is later determined that I did speak to another person about the test before the instructor said it was allowed, I will be brought before the Undergraduate Judicial Board and, if found responsible for academic dishonesty or academic contempt, fail the class.

Signature:_____

Instructions for Written and Discussion Sections

There are some problems that require you to describe a controller, or to report values from a design or a simulation, or to explain why you expect the second-order assumption to work or not. Be sure to indicate which part of a problem you are answering and put your name on the paper. As always, only put answers to one problem on a page. Note that there is a "summary page" for each problem where you will record information such as controller gains, closed-loop poles and zeros, and transient response characteristics.

Instructions for Computer-Based Sections

All your files for this test will be placed in a directory on your OIT account. There are two scripts you will be running to set everything up. The first - `StartTest3` - will create a folder called `ECE141TEST3` in your account and then set the permissions such that I can look at the files. You *must* make sure all your scripts, worksheets, and graphs end up in this folder. The second - `EndTest3` - will send me a snapshot of the directory contents and lock the directory from further changes. After I receive the e-mail, I will copy the directory contents to another location and delete the originals. Be sure to use the stated names for files in those problem parts requiring JPEG images.

To run the `StartTest3` script, log into your UNIX account and type:

```
~mrg/public/ECE141S07/StartTest3
```

Similarly, when you are finished and ready to lock your directory, type:

```
~mrg/public/ECE141S07/EndTest3
```

Also see the next page for instructions on creating and saving plots.

Titling, Naming, and Saving Files

For this test, in order to conserve space, you will be using the JPEG format instead of PostScript. The following instructions will lead you through the process of saving both root locus plots and LTIview plots.

Root Locus Plots

First, get the plot where it needs to be with respect to showing the locus and having the closed-loop poles at the appropriate locations. Also make sure that your compensator - if there is one - is given in zpk format by going to `Edit->SISOTool Preferences`, selecting the `Options` tab, and switching the `Compensator Format` to `Zero/pole/gain`. Then:

(a) Turn *off* the Open-Loop Bode if need be from the `View` menu so that only the *Root Locus Editor* is showing.

(b) Right-click inside the whitespace in the editor plot and bring up the `Properties` menu.

(c) Within the `Labels` tab, change the title making sure to include the problem part and your NET ID. For example, for the first root locus, change the title to `Root Locus Problem 1a (NETID)`.

(d) Go to the `File` menu and select `Save Session`. When the box comes up, give the session the name of the problem you are working on - for example `Problem1a`. This will save the information contained within the Root Locus in a way that can be retrieved later should something happen to the plot file.

(e) Again go to the `File` menu, and select `Print to Figure`. This will bring up a figure window containing the same information as the Root Locus editor plot, including the figure title.

(f) Within the `File` menu of the *figure* window, select `Save As`. In the `Save As` box, change the `Save as type` to `JPEG image (*.jpg)` and save the file with the name given in that portion of the test. For example, for the first root locus of Problem 1, you would use `RootLocus1a.jpg`.

LTI Viewer Plots

First, get the plot where it needs to be with respect to showing the relevant characteristics (OS%, settling time, and steady state values). Also be sure to turn *off* the `Closed Loop: r to u (green)` system. Then:

(a) Right-click inside the whitespace in the response plot and bring up the `Properties` menu.

(b) Within the `Labels` tab, change the title making sure to include the problem part and your NET ID. For example, for the first step response, change the title to `Step Response Problem 1a (NETID)`.

(c) Go to the `File` menu of the LTI Viewer and select `Print to Figure`. This will bring up a figure window containing the same information as the viewer, including the figure title.

(d) Within the `File` menu of the *figure* window, select `Save As`. In the `Save As` box, change the `Save as type` to `JPEG image (*.jpg)` and save the file with the name given in that portion of the test. For example, for the first step response of Problem 1, you would use `StepResponse1a.jpg`.

Name (please print):
Community Standard (print ACPUB ID):

Problem I: [50 pts.] System I

Given the block diagram of a control system in Figure 1.6b on p. 12, where the Input Transducer and Output Transducer are both unity, the frequency model of the controller is initially some constant K, and the frequency model of the plant is

$$G = \frac{s+20}{(s+1)(s+5)(s+7)(s+9)}$$

Gain Control

(a) Generate a root locus plot for $K > 0$.

(b) Assume that you want the system to have a step response with an OS% of 16 ($\zeta \approx 0.5$). Determine the gain value K to accomplish this design point and call this System 1a. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system, the values of the static error constant of position and steady state error for a step input, and the OS% and settling time predicted using the second-order assumption. Note - some of this is already done.

(c) Using the information in the introduction to the test, change the root locus plot title to "Root Locus Problem 1a (NETID)" where `NETID` is your NETID and save the file as `RootLocus1a.jpg`.

(d) Generate a simulation of the step response and label the simulated values of OS%, settling time, and steady state response. Then change the plot title to "Step Response Problem 1a (NETID)" and save it as a JPEG file called `StepResponse1a.jpg`. Find and record the simulated values for steady state position error, OS%, and settling time on the summary sheet, then state if the transient characteristics match well with your design values and why that might be the case.

Transient Response Design

(e) Now assume that you want the system to have the same OS% but you need it to settle twice as fast as System 1a - this will be System 1b. Graphically determine the transfer function of a lead controller that will allow this to happen while likely satisfying the second-order assumptions. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system, the values of the static error constant of position and steady state error for a step input, and the OS% and settling time predicted using the second-order assumption.

(f) Leaving the gain set to achieve the design point, change the root locus plot title to "Root Locus Problem 1b (NETID)" and save the file as `RootLocus1b.jpg`.

(g) Generate a simulation of the step response and label the simulated values of OS%, settling time, and steady state response. Then change the plot title to "Step Response Problem 1b (NETID)" and save it as a JPEG file called `StepResponse1b.jpg`. Find and record the simulated values for steady state position error, OS%, and settling time on the summary sheet, then state if the transient characteristics match well with your design values and why that might be the case.

Steady State Error Correction

(h) Design a passive compensator to place in series with the one above to reduce the steady state error found by a factor of 10 - this will be System 1c. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system and the values of the static error constant of position and steady state error for a step input.

(i) Leaving the gain set to achieve this final design point, change the root locus plot title to "Root Locus Problem 1c (NETID)" and save the file as `RootLocus1c.jpg`.

(j) Generate a simulation of the step response and label the simulated value of the steady state response. Then change the plot title to "Step Response Problem 1c (NETID)" and save the file as `StepResponse1c.jpg`. Find and record the simulated values for steady state position error, and overall settling time on the summary sheet, then state if the steady state error matches well with your design value and why that might be the case.

Summary Sheet - Problem 1

Design Values

Sys.	Controller	CL Poles	CL Zeros	K_p	$e_{\text{step}}(\infty)$	OS%	t_s
1a						16	
1b						16	
1c						N/R	N/R

Simulation Values

Sys.	$e_{\text{step}}(\infty)$	OS%	t_s
1a			
1b			
1c		N/R	N/R

Discussion

Name (please print):
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Problem II: [50 pts.] System II

Given the block diagram of a control system in Figure 1.6b on p. 12, where the Input Transducer and Output Transducer are both unity, the frequency model of the controller is initially some constant K, and the frequency model of the plant is

$$G = \frac{1}{(s)(s+10)}$$

Gain Control

(a) Generate a root locus plot for $K > 0$.

(b) Assume that you want the system to have a step response with a damped frequency of 10 rad/s. Determine the gain value K to accomplish this design point and call this System 2a. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system, the values of the static error constant of velocity and steady state position error for a ramp input, and the OS% and settling time for a step response predicted using the second-order assumption.

(c) Using the information in the introduction to the test, change the plot title to "Root Locus Problem 2a (NETID)" where `NETID` is your NETID and save the file as `RootLocus2a.jpg`.

(d) Generate a simulation of the step response and label the simulated values of OS%, settling time, and steady state response. Then change the plot title to "Step Response Problem 2a (NETID)" and save it as a JPEG file called `StepResponse2a.jpg`. Find and record the simulated values for OS% and settling time on the summary sheet, then state if the transient characteristics match well with your design values and why that might be the case.

(e) Given that this is a Type I system, generate a simulation of the ramp response and label a value to help you determine the steady state position error for a ramp input. Then change the plot title to "Ramp Response Problem 2a (NETID)" and save it as a JPEG file called `RampResponse2b.jpg`. Find and record the simulated value for steady state position error.

Transient Response Design

(f) Now assume that you want the system to have a settling time of 0.5 sec and a damping ratio of 0.6 - this will be System 2b. Graphically determine the transfer function of a PD controller that will allow this to happen. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system, the values of the static error constant of velocity and steady state position error for a ramp input, and the OS% and settling time predicted using the second-order assumption.

(g) Leaving the gain set to achieve the design point, change the root locus plot title to "Root Locus Problem 2b (NETID)" and save the file as `RootLocus2b.jpg`.

(h) Generate a simulation of the step response and label the simulated values of OS%, settling time, and steady state response. Then change the plot title to "Step Response Problem 2b (NETID)" and save it as a JPEG file called `StepResponse2b.jpg`. Find and record the simulated values for OS% and settling time on the summary sheet, then state if the transient characteristics match well with your design values and why that might be the case.

(i) Given that this is a Type I system, generate a simulation of the ramp response and label a value to help you determine the steady state position error for a ramp input. Then change the plot title to "Ramp Response Problem 2b (NETID)" and save it as a JPEG file called `RampResponse2b.jpg`. Find and record the simulated value for steady state position error.

Steady State Error Correction

(j) Design an active compensator to place in series with the one above to raise the system type - this will be System 2c. Record the transfer function for the controller and determine the locations of the closed loop poles and zeros of the overall system and the values of the static error constant of velocity and steady state position error for a ramp input.

(k) Leaving the gain set to achieve this final design point, change the root locus plot title to "Root Locus Problem 2c (NETID)" and save the file as `RootLocus2c.jpg`.

(l) Generate a simulation of the step response and label the simulated value of the steady state response. Then change the plot title to "Step Response Problem 1c (NETID)" and save the file as `StepResponse1c.jpg`.

(m) Generate a simulation of the ramp response and label a value to help you determine the steady state position error for a ramp input. Then change the plot title to "Ramp Response Problem 2c (NETID)" and save it as a JPEG file called `RampResponse2c.jpg`. Find and record the simulated value for steady state position error.

Summary Sheet - Problem 2

Design Values

Sys.	Controller	CL Poles	CL Zeros	K_v	$e_{\text{ramp}}(\infty)$	OS%	t_s
1a							
1b							
1c						N/R	N/R

Simulation Values

Sys.	$e_{\text{ramp}}(\infty)$	OS%	t_s
1a			
1b			
1c		N/R	N/R

Discussion